IN THE CLAIMS

Each claim of the present application is set forth below with a parenthetical notation immediately following the claim number indicating the current claim status. The Examiner's entry of the claim amendments, as shown in marked-up form, under Section 1.121 is respectfully requested.

1. (Currently Amended) An integrated circuit structure comprising:

a semiconductor layer having a major surface formed along a plane;

a first and a second spaced-apart doped region formed in the surface;

an isolation region disposed overlying and between said first and said second regions for electrically insulating said first and said second regions;

a plurality of layers overlying said ~~first and said second doped regions~~ isolation region, including a first and a second trench therein, wherein said first and said second trenches extend through said isolation region;

a third doped region formed in said first trench over said first doped region, and of a different conductivity type than said first doped region;

a fourth doped region formed in said second trench over said second doped region, and of a different conductivity type than said second doped region;

a first oxide layer proximate said third doped region; and

a second oxide layer proximate said fourth doped region.

2. (Currently amended) The integrated circuit structure of claim 1 wherein the first doped region is a first source/drain region of a first MOSFET and the third doped region is a channel region of the first MOSFET, and wherein the second ~~third~~ doped region is a first source/drain region of a second MOSFET and the fourth doped region is a channel region of the second MOSFET.

3. (Original) The integrated circuit structure of claim 2 wherein the first and the second MOSFETs form a complimentary MOSFET pair of transistors.

4. (Original) The integrated circuit structure of claim 1 wherein the isolation region comprises a trench of electrically insulating material disposed between the first and the second doped regions and a layer of electrically insulating material overlying the first and the second doped regions.

5. (Original) The integrated circuit structure of claim 1 wherein the material of the isolation region comprises an electrically insulating material.

6. (Original) The integrated circuit structure of claim 1 wherein the material of the isolation region comprises silicon dioxide.

7. (Currently amended) The integrated circuit structure of claim 1 wherein one of the plurality of layers is removed to expose a portion of ~~over~~ the third doped region in the first trench and a portion of the fourth doped region in the second trench, and wherein the first oxide layer is proximate said exposed portion of the third doped region, and wherein the second oxide layer is proximate said exposed portion of the fourth doped region.

8. (Original) The integrated circuit structure of claim 1 further comprising:

a fifth doped region overlying the first doped region and of the same conductivity type as the first doped region, wherein the first doped region is a first source/drain region of a first MOSFET, and wherein said fifth doped region is a second source/drain region of said first MOSFET, and wherein the third doped region is a channel region of said first MOSFET.

a sixth doped region overlying the second doped region of the same conductivity type as the second doped region, wherein the second doped region is a first source/drain region of a second MOSFET, and wherein said sixth doped region is a second source/drain region of said second MOSFET, and wherein the fourth doped region is a channel region of said second MOSFET; and wherein the first oxide layer is a gate oxide layer of said first MOSFET.

wherein the second oxide layer is a gate oxide layer of said second MOSFET.

9. (Original) The integrated circuit structure of claim 8 further comprising:

a first and a second conductive element adjacent the first and the second gate oxide layers, respectively, to control operation of the respective first and the second MOSFETs.

10. (Original) The integrated circuit structure of claim 9 wherein the first and the second conductive elements comprise polysilicon and operate as the gate for the first and the second MOSFETs, respectively.

11. (Original) The integrated circuit structure of claim 8 further comprising a third conductive element electrically connecting the first and the second source/drain regions.

12. (Original) The integrated circuit structure of claim 1 wherein at least one of the plurality of layers comprises a doped insulating layer for serving as a dopant source to diffuse dopants into the third and the fourth doped regions.

13. (Original) The integrated circuit structure of claim 12 wherein the third and the fourth doped regions each form a channel region, and wherein the dopants diffused from the doped insulating region form source/drain extensions within each of the channel regions.

14. (Currently Amended) An integrated circuit structure comprising:

a semiconductor layer having a major surface formed along a plane;

a first and a second doped source/drain region formed in the major surface;

an isolation region disposed overlying and between said first and said second source/drain regions for electrically insulating said first and said second source/drain regions;

a plurality of layers overlying said first and said ~~second source/drain regions~~ isolation region, including a first and a second trench formed therein, wherein said first and said second trenches extend through said isolation region;

a first doped channel region formed in said first trench overlying said first source/drain region and having a different conductivity type than said first source/drain region;

a second doped channel region formed in said second trench overlying said second source/drain region and having a different conductivity type than said second source/drain region;

a third and a fourth doped spaced-apart source/drain region, wherein said third source/drain region is vertically aligned with said first channel region and said first source/drain region, and wherein said fourth source/drain region is vertically aligned with said second source/drain region and said second channel region, and wherein said third source/drain region is of the same conductivity type as the first source/drain region, and wherein said fourth source/drain region is of the some conductivity type as said second source/drain region;

a first oxide layer proximate said first channel region ~~regions~~, and

a second oxide layer proximate said second channel region.

15-24 (Withdrawn)